Notice of References Cited	Application/Control No. 10/749,206	Applicant(s)/Patent Under Reexamination CHOI, KEE-HOON	
	Examiner Biju Chandran	Art Unit 2835	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
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FOREIGN PATENT DOCUMENTS

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	N					
	O					
	P					
	Q					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Pradeep Lal, Packaging Reliability, Chip-Scale Semiconductor, Package Architecture – An Overview, Wiley Encyclopedia of Electrical and Electronics Engineering, John Wiley and Sons, 1999, pages 516-518
	V	
	W	
	X	

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